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<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(use as many sheets as necessary)</p>				<p><i>Complete if Known</i></p>	
Sheet	1	of	3	Application Number	
				Filing Date	
				First Named Inventor	Marius K. Orłowski
				Group Art Unit	
				Examiner Name	
				Attorney Docket Number	SC12885TP

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner Signature	By Review	Date Considered	02/27/05
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) Sheet 2 of 3				<i>Complete if Known</i>	
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				Examiner Name	
Attorney Docket Number		SC12885TP			

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
BR	AH	MONFRAY, S. et al; "50nm-Gate All Around (GAA)-Silicon On Nothing (SON)-Devices: A Simple Way to Co-Integration of GAA Transistors Within Bulk MOSFET Process"; 2002 Symposium on VLSI Technology; 2002; pp 108-109; 2002 Symposium on VLSI Technology Digest of Technical Papers	
BR	AI	MONFRAY, S. et al.; "Highly-Performant 38nm SON (Silicon-On-Nothing) P-MOSFETs with 9nm-thick Channels"; 2002 IEEE International SOI Conference; 10/02; pp 20-22	
BR	AJ	MONFRAY, S. et al.; " SON (Silicon-On-Nothing) P-MOSFETs with Totally Silicided (CoSi ₂) Polysilicon on 5nm-thick Si Films: The Simplest Way to Integration of Metal Gates on Thin FD Channels"; IEDM; 2002; pp 263-266; IEEE	
BR	AK	YU, Bin et al; "FinFET Scaling to 10nm Gate Length"; IEDM; 2002; pp 251-254; IEEE	
BR	AL	KEDZIERSKI, Jakub et al.; "High_Performance Symmetric-Gate and CMOS-Compatible V _t Asymmetric-Gate FinFET Devices"; IEEE; 2001; 4 pp	
BR	AM	CHOI, Y. et al.; "Sub-20nm CMOS FinFET Technologies"; IEDM; 2001; pp 19.1.1-19.1.4; IEEE	
BR	AN	KIM, K. et al.; "Double-Gate CMOS: Symmetrical-Versus Asymmetrical-Gate Devices"; IEEE Transactions on Electron Devices; February, 2001; pp 294-299; Vol 48, No 2; IEEE	
BR	AO	MONFRAY, S. et al.; "First 80nm SON (Silicon-On-Nothing) MOSFETs With Perfect Morphology and High Electrical Performance"; IEDM; 2001; pp 29.7.1-29.7.4; IEEE	
BR	AP	HISAMOTO, D. et al.; "FinFET-A Self-Aligned Double-Gate (MOSFET) Scalable to 20nm"; IEEE Transactions of Electron Devices; December 2000; pp 2320-2325; Vol 47, No 12; IEEE	

Examiner Signature	<i>Br. Ken</i>	Date Considered	02/27/05
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Sheet	3	of	3	Attorney Docket Number
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	²
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<i>JK</i>	AQ	JURCZAK, M. et al.; "Silicon-on-Nothing (SON) – an Innovative Process for Advanced CMOS"; IEEE Transactions on Electron Devices"; November, 2000; pp 2179-2187; Vol 47, No 11; IEEE	
<i>JK</i>	AR	FOSSUM, J.G. et al.; "Extraordinarily High Drive Currents in Asymmetrical Double-Gate MOSFETs"; Superlattices and Microstructures; 2000; pp 525-530; Vol 28; No 5/6; Academic Press	
<i>JK</i>	AS	JURCZAK, M. et al.; "SON (Silicon on Nothing) – A New Device Architecture for the ULSI Era"; Symposium of VLSI Technology Digest of Technical Papers; 1999; pp 29-30	
<i>JK</i>	AT	HUANG, X. et al.; "Sub 50-nm FinFET: PMOS"; IEDM; 1999; pp 3.4.1-3.4.4; IEEE	
<i>JK</i>	AU	HISAMOTO, D. et al.; "A Folded-Channel MOSFET for Deep-sub-tenth Micron Era"; IEDM; 1998; pp 1032-1034; IEDM	
<i>JK</i>	AV	TANAKA, T. et al.; "Ultrafast Operation of V_{th} -Adjusted p^+ - n^+ Double-Gate SOI MOSFET's"; IEEE Electron Device Letters; October 1994; pp 386-388; Vol 15, No 10; IEEE	
<i>JK</i>	AW	International Search Report	
<i>JK</i>	AX	Specification, abstract and drawings for Application No. 10/074,732 Filed February 13, 2002	

Examiner Signature	<i>Bru. Raman</i>	Date Considered	<i>02/27/05</i>
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